EXORciser Bus Signals

The EXORciser bus interfaces the MPU Module with other modules being used in the EXORciser. This bus permits the EXORciser to be configured to meet a user's specific application.

Data Bus (D0-D7) – These eight bi-directional lines, when enabled, provide a two-way transfer of data between the MPU Module and the selected memory location. The data bus drivers on the modules are three-state logic devices.

Address Bus (A0-A15) – These 16 lines, when enabled, transfer the MPU memory address to the selected memory location. The MPU Module controls the operation of these lines through its three-state bus drivers.

Read/Write (R/W) – This MPU output signal indicates whether the MPU Module is performing a memory read (high) or write (low) operation. The normal standby state of this line is read (high). Also, when the MC6800 MPU on the module is halted, this signal will be in the read state.

Valid Memory Address (VMA) – This line, when high. indicates that the address on the bus is valid.

Valid User's Address (VUA) – This line, when high, indicates that the address on the address bus is valid and the EXORciser is not addressing its EXbug program.

Memory Clock (MEMCLK) – This is the basic clock signal used by the MPU Module to generate its $\phi 1$ and $\phi 2$ non-overlapping clock signals.

Phase 1 ($\phi 1$) Clock – This signal is derived from the Memory Clock and is present during the MPU addressing time. This signal is controlled by the MPU Module.

Phase 2 ($\phi 2$) Clock – This signal also is derived from the Memory Clock and used to synchronize the transfer of data on the data bus. This signal is controlled by the MPU Module.

Bus Available (BA) – The Bus Available signal will normally be a low level. When activated, it will go high indicating that the address bus is available. This will occur if the Halt line is low or the MC6800 MPU is in the WAIT state as the result of executing a WAI instruction. At such time, all the MPU Module three-state output drivers will go to their off state and other outputs to their normally inactive state. An interrupt command or actuating the ABORT or RESTART switch removes the MPU from the WAIT state.

Interrupt Request (IRQ) – This level sensitive input, on going low, requests that an interrupt sequence be generated in the MC6800 MPU. The MPU will wait until it completes the current instruction that it is executing before it recognizes this request. At that time, if the interrupt mask bit in the MPU Condition Code Register is not set, the MPU will begin the interrupt sequence.

Non-Maskable Interrupt (NMI) – This level sensitive input, on going low, requests that an interrupt sequence be generated within the MC6800 MPU. The MPU will wait until it completes the current instruction that it is executing before it recognizes this request. At that time, the MPU will begin its non-maskable interrupt routine.

Reset – This edge sensitive signal initiates an MC6800 MPU power-on vectored interrupt initialize routine when power is first applied to the EXORciser and each time the EXORciser's RESTART switch is actuated. This signal, in addition to resetting the module's MPU, is used to reset and initialize the rest of the EXORciser.

Three-State Control (TSC) – This input, when high, causes all of the MPU Module's Address Bus lines and R/W line to go to their off or high-impedance state. The Valid Memory Address and Valid User's Address signal will be forced low. The Data Bus is not affected by the Three-State Control. This signal is initially jumpered to ground on the MPU Module.

Refresh Request (REFREQ) – This signal, when low, initiates a memory refresh operation. The MPU Module, on receiving this input, stops generating the $\phi 1$ and $\phi 2$ clock signals with $\phi 1$ high and, through the Refresh Grant command, instructs the initiating memory module to refresh itself.

Refresh Grant (REFGRANT) – The MPU Module, on receiving a Refresh Request input, generates a Refresh Grant signal to instruct the initiating module to refresh itself.

Memory Ready (MEMRDY) – This signal enables the MPU Module to work with slow memories. The MPU Module, on receiving a low level Memory Ready input, stops generating the $\phi 1$ and $\phi 2$ clock signals with $\phi 2$ high. The initiating module, on completing its memory operation, returns the Memory Ready signal to a high level.

Halt – When this input is low, all activity in the MC6800 MPU will be halted. This input is level sensitive. In the MC6800 MPU will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction, Bus Available will be high, Valid Memory Address and Valid User's Address will be low, and all other three-state lines will be in their off or high-impedance state.

Transition of the Halt line must not occur during the last 250 ns of $\phi 1$. To insure single instruction operation, the Halt line must go high for one $\phi 1$ clock pulse.

Refresh Clock (REFCLK) – This signal is generated by the dynamic memory module being used as the master refresh module. This signal is used to initiate a memory refresh operation on the dynamic modules functioning as slave refresh modules.

Stand By (STDBY) – This line is a low level during a power-fail condition and a high level during normal EXORciser operation.

Bus Control

It is possible for a module other than the MPU Module to gain control of the bus. This module would place a low level Halt on the bus and monitor the Bus Available signal. When the MPU Module completes the instruction it is performing, it generates a high level Bus Available signal. The module requesting control of the bus now must pull the Three-State Control line low, forcing the MPU Module address bus drivers to their high-impedance state. The requesting module now has control of the EXORciser bus until it elects to relinquish control.