MOTOROLA

MSET30(D1)

EXORset 30

User's Guide

MICROSYSTEMS

CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

The EXORset is a cost-effective, compact, powerful development tool used in the design and development of microcomputer systems.

The EXORset is made up of seven distinct functional units :

- The EXORset Main Controller Board.
- The 9" CRT.
- The dual mini-floppy assembly.
- The Floppy Disk Controller and 16K-byte RAM board.
- The ASCII keyboard and function keys assembly.
- The power supply unit.
- The enclosure.

Figure 1-1. Typical EXORset System

1.2 SPECIFICATIONS

The specifications of the various functional units are identified in the following paragraphs.

1.2.1 Main Controller Board Specifications

Power requirements (max)	5V/6A, +12V/1A, -12V/1A
Operating temperature	0 to 50 deg.C
Processor	MC6809
Word size	
Data	8 bits
Address	16 bits
Instructions	8, 16, 24, 32 bits
Instructions	59 instruction mnemonics
Addressing modes	10
Clock cycle time	1 microsecond
Baud rates	110 - 2400
Memory size	up to 32K bytes of RAM and up to 24K bytes of EROM available to user.
Serial interface	
Input	EIA RS-232C
Output	EIA RS-232C
Physical Characteristics	
Dimensions (WxD)	9.76 in. (248 mm) x 19.84 in. (504 mm)
Board thickness	.063 in. (1.6 mm)
I/O connectors	
Parallel interface	50-pin card edge connector
Serial interface	20-pin card edge connector
Cassette	5-pole DIN connector
CRT	Coax connector
Keyboard	ASCII: flex-tail, 23-pin or card edge, 50-pin
	Function keys: flex-tail, 8-pin or card edge, 20-pin

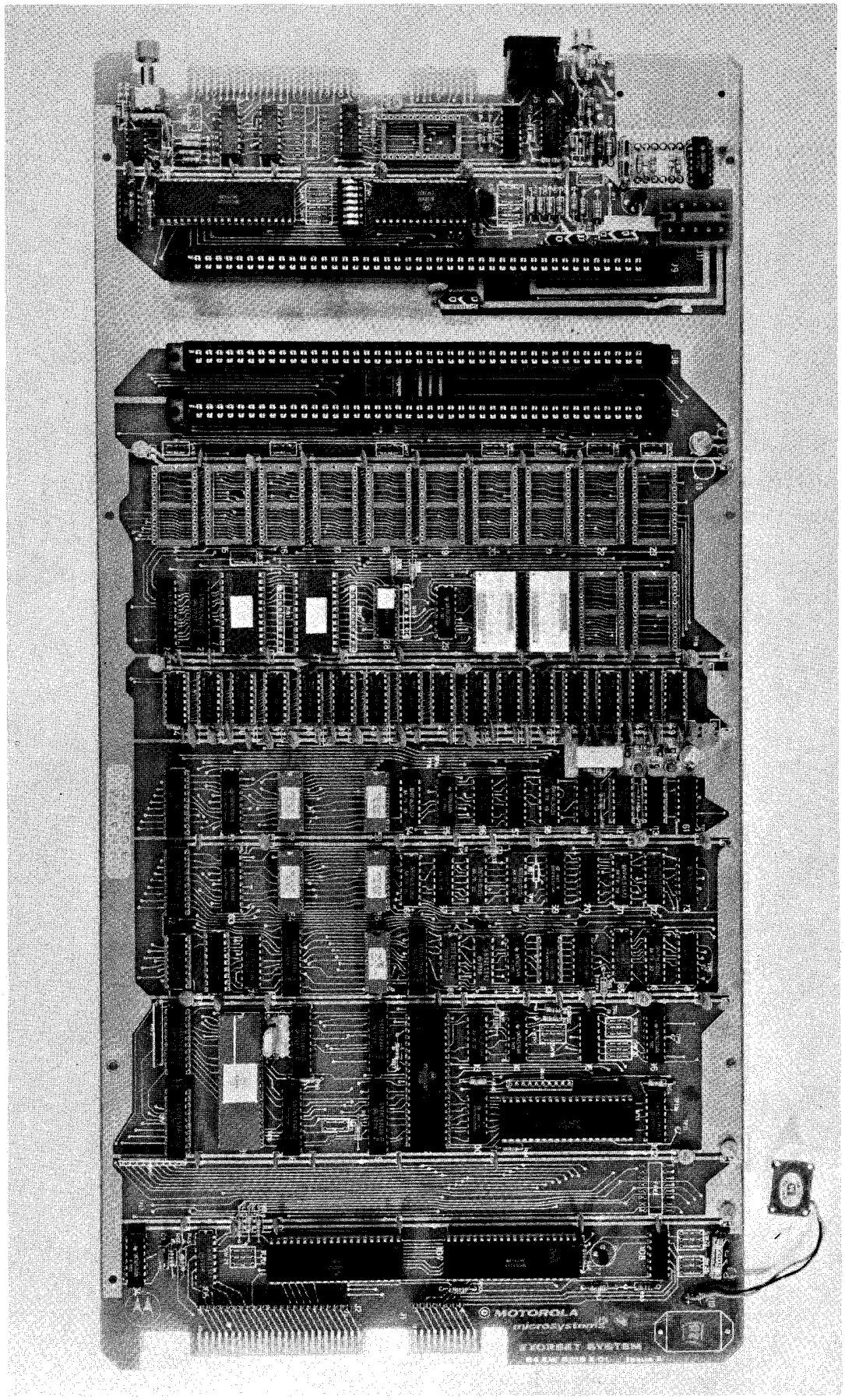


FIGURE 1-2. Main Controller Board

1.2.2 Floppy Disk Controller Board Specifications

Power requirements (max)	5V/0.8A, +12V/0.2A, -12V/0.15A
Operating temperature	0 to 50 deg.C
Memory size	16K bytes of RAM, 1K bytes of EROM (disk driver)
Interface	
Output	TTL open collector
Input	220/330 ohm line terminations
Physical characteristics	
Dimensions (WxD)	9.76 in. (248 mm) x 5.75 in. (146 mm)
Board thickness	.063 in. (1.6 mm)
Connector, I/O	34-pin card edge connector
Connector, bus	86-pin card edge connector

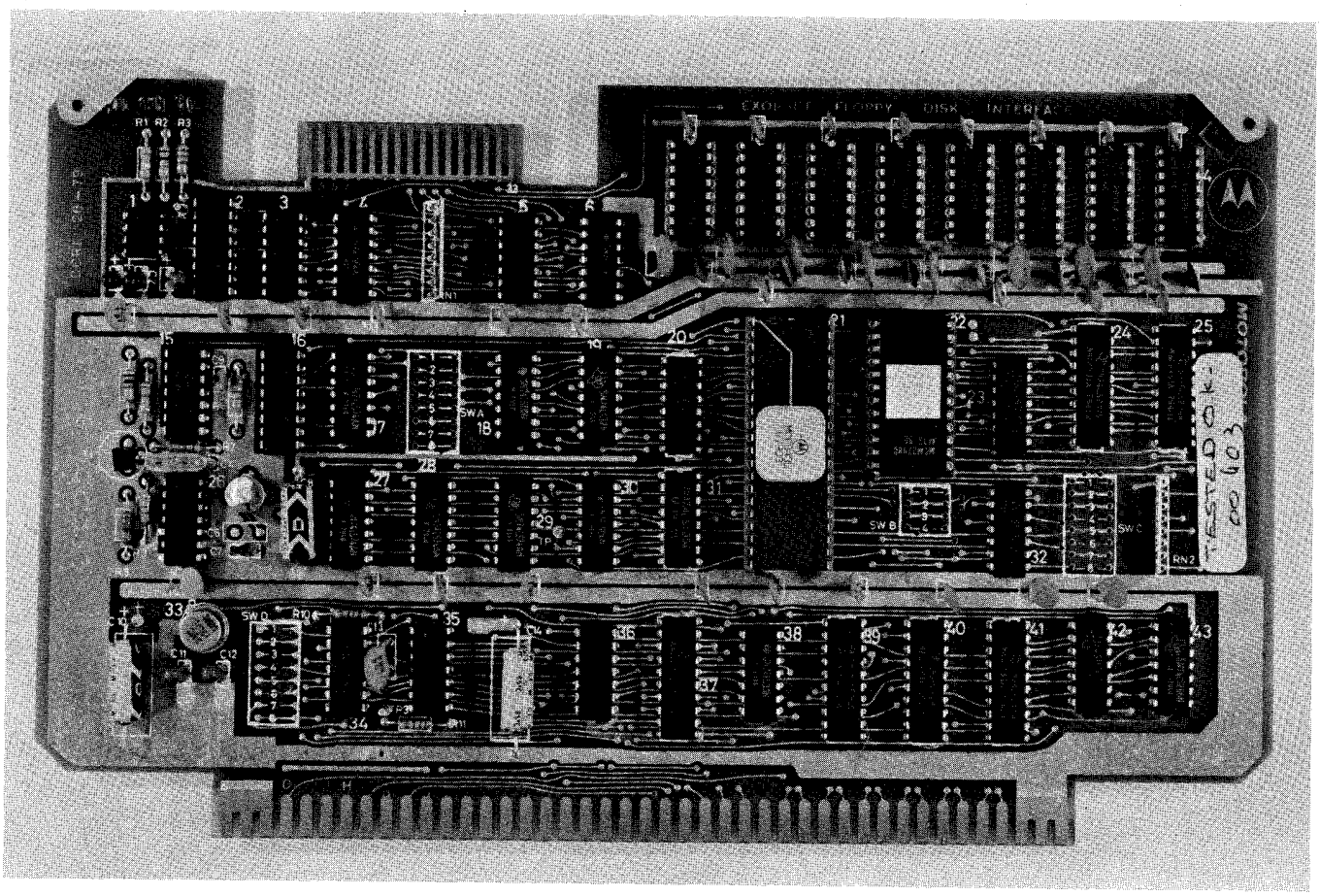


Figure 1-3. Floppy Disk Controller Board

TABLE 2-1. EXORset Expansion Bus Signals (J7,J8,J9)

PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
A	+5 Vdc	+5 Vdc POWER - Used for the system logic circuits and available to the user for prototype module requirements (10 amps tot. max).
B	+5 Vdc	+5 Vdc POWER - Same as above.
C	+5 Vdc	+5 Vdc POWER - Same as above.
D	IRQnot	INTERRUPT REQUEST - A low level sensitive input signal to the MPU used to request generation of an MPU interrupt sequence. This signal is latched every cycle during Q high, but will not be received by the MPU until the following bus cycle. At that time, if the interrupt mask bit in the MPU Condition Code Register is not set, the MPU will begin executing the interrupt sequence.
E	NMInot	NON-MASKABLE INTERRUPT - A low going edge sensitive input signal to the MPU used to request generation of a MPU non-maskable interrupt sequence. When sampled low one cycle after being sampled high (samples taken every cycle during Q high), an NMI will be triggered. The MPU will recognize the signal on the following bus cycle and begin á non-maskable interrupt sequence at that time, regardless of the logic state of the Interrupt Mask Bit in the MPU Condition Code Register.
F	VMA	VALID MEMORY ADDRESS - This signal is connected to +5V in the EXORset.
H	---	NOT USED - Reserved for system expansion.
J	E	E - Clock signal generated by the clock circuitry on the EXORset Main Controller Board. E is similar to phase 2 clock in 6800 systems. Data is placed on the bus during E.
K	GND	GROUND - Power ground for +/- 12 Vdc.
L	MEMCLK	MEMORY CLOCK - Ungated, TTL level clock signal, in phase with E.
M	-12Vdc	-12 Vdc POWER - Used for system logic and available to the user for custom designed prototype modules (1.0 A max).
N	---	NOT USED
P	BA	BUS AVAILABLE - This signal, decoded with Bus Status (BS) indicates the MPU state : BA BS 0 0 Normal 0 1 Interrupt Acknowledge 1 0 Sync. Acknowledge 1 1 Halt or Bus Grant
R	MEMRDY	MEMORY READY - Not used in the EXORset.

Table 2-1. EXORset Expansion Bus Signals (J7,J8,J9) (cont'd)

PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
S	LIC	LAST INSTRUCTION CYCLE - Not used in the EXORset.
T	+12Vdc	+12 Vdc POWER - Used for the system logic and available to the user for custom designed prototype modules (5.0 A max).
U	STANDBY	STANDBY POWER - Not used in the EXORset.
V	PWRFAIL	POWER FAIL - Not used in the EXORset
W	PARITY	PARITY ERROR - Not used in the EXORset.
X	GND	GROUND
Y	GND	GROUND
Z	GND	GROUND
Anot	FIRQnot	FAST INTERRUPT - A low level sensitive input to the MPU used to request generation of an MPU fast interrupt sequence. The MPU will wait until it completes the instruction being executed before it recognizes the request. At that time, if the fast interrupt mask bit in the MPU Condition Code Register is not set, the MPU will begin executing the fast interrupt sequence.
Bnot	GND	GROUND
Cnot	RASnot	ROW ADDRESS STROBE - This signal, generated by the EXORset Main Controler Board is used to control the 16K RAM block located on the Floppy-Disk Controller Board. This signal is only connected to the first (J07) bus expansion connector.
Dnot	CASnot	COLUMN ADDRESS STROBE - Same as RAS above.
Enot	EAHL	ADDRESS HIGH/LOW - Same as RAS above .
Fnot	---	USER DEFINED - This signal may be used for custom modules.
Hnot	D3not	DATA (bit 3) - One of 8 bi-directional data lines used to provide a two-way data transfer between the MPU and all other plug-in modules within the system. The data bus drivers on the other modules are in their off or high impedance state except when selected during a memory read or write operation.
Jnot	D7not	DATA (bit 7) - Same as D3not on pin Hnot.
Knot	D2not	DATA (bit 2) - Same as D3not on pin Hnot.
Lnot	D6not	DATA (bit 6) - Same as D3not on pin Hnot.
Mnot	A14	ADDRESS (bit 14) - One of the 16 address lines from the MPU that permits the MPU to select any addressable memory location within the EXORset.

TABLE 2-1. EXORset Expansion Bus Signals (J7,J8,J9) (cont'd)

PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
Nnot	A13	ADDRESS (bit 13) - Same as A14 above.
Pnot	A10	ADDRESS (bit 10) - Same as A14 above.
Rnot	A9	ADDRESS (bit 9) - Same as A14 above.
Snot	A6	ADDRESS (bit 6) - Same as A14 above.
Tnot	A5	ADDRESS (bit 5) - Same as A14 above.
Unot	A2	ADDRESS (bit 2) - Same as A14 above.
Vnot	A1	ADDRESS (bit 1) - Same as A14 above.
Wnot	GND	GROUND
Xnot	GND	GROUND
Ynot	GND	GROUND
1	+5 Vdc	+5 Vdc POWER - Used for the system logic circuits and available to the user for prototype module requirements (10 A total max).
2	+5 Vdc	+5 Vdc POWER - Same as above.
3	+5 Vdc	+5 Vdc POWER - Same as above.
4	G/H	GO/HALT - When this input to the MPU is in the high state, the MPU will fetch the instruction addressed by the program counter and start instruction execution. When low, all activity in the MPU will be halted. This input is level sensitive.
5	RESETnot	RESET - This buffered input signal to the MPU is used to restart the EXORset when power is initially applied. Restart occurs on the low-to-high transition of the RESTART signal. If the RESTART pushbutton switch, located on the Main Controller Board, is depressed while the system is operating, the low-to-high transition of the RESET signal will cause the MPU to execute the EXORbug restart routine or the restart routine indicated by the user.
6	R/W	READ/WRITE - This signal is generated by the MPU and indicates to the other modules contained within the system that the MPU is performing a memory read (high) or write (low) operation. The normal standby state of this signal is read (high). Additionally, when the MPU is halted, this signal will be in the read state.
7	Q	Q - A quadrature clock signal generated by the MPU which leads the E (enable) signal. Addresses from the MPU will be guaranteed valid with the leading edge of Q.

TABLE 2-1. EXORset Expansion Bus Signals (J7,J8,J9) (cont'd)

PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
8	GND	GROUND - Power ground for +/-12Vdc.
9	GND	GROUND - Power ground for +/-12Vdc.
10	VUA	VALID USER'S (ALTERNATE MAP) ADDRESS - This signal, when high, allows additional module(s) to respond in address map 2 .
11	-12Vdc	-12Vdc POWER - Used for the system logic circuits and available to the user for custom designed prototypes modules (1.0 A max).
12	REFREQ	REFRESH REQUEST - Not used in the EXORset. Due to its design concept, the EXORset does not provide the capability of stretching the clock, thus does not allow the use of cycle stealing mode of dynamic memory refresh .
13	REFGNT	REFRESH GRANT - Same remark as above.
14	DEBUG	DEBUG - Not used in the EXORset.
15	TSG	THREE-STATE GRANT - Not used in the EXORset.
16	+12Vdc	+12Vdc POWER - Used for the system logic circuits and available to the user for prototype module requirements.
17	STANDBY	STANDBY POWER - Not used in the EXORset.
18	CLOCK	CLOCK - Not used in the EXORset.
19	VXA	VALID EXECUTIVE (ALTERNATE MAP) ADDRESS - This signal, when high, allows additional module(s) to respond in address map 1.
20	GND	GROUND
21	GND	GROUND
22	GND	GROUND
23	BS	BUS STATUS - This signal, decoded with Bus Available (BA) indicates the MPU state : BA BS 0 0 Normal 0 1 Interrupt Acknowledge 1 0 Sync. Acknowledge 1 1 Halt or Bus Grant
24	GND	GROUND
25	---	USER DEFINED - This signal line may be used for custom modules.
26	---	USER DEFINED - Same as above.

TABLE 2-1. EXORset Expansion Bus Signals (J7,J8,J9) (cont'd)

PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
27	---	USER DEFINED - Same as above.
28	---	USER DEFINED - Same as above.
29	D1not	DATA (bit 1) - Same as D3not on pin Hnot.
30	D5not	DATA (bit 5) - Same as above.
31	D0not	DATA (bit 0) - Same as above.
32	D4not	DATA (bit 4) - Same as above.
33	A15	ADDRESS (bit 15) - Same as A14 on pin Mnot.
34	A12	ADDRESS (bit 12) - Same as above.
35	A11	ADDRESS (bit 11) - Same as above.
36	A8	ADDRESS (bit 8) - Same as above.
37	A7	ADDRESS (bit 7) - Same as above.
38	A4	ADDRESS (bit 4) - Same as above.
39	A3	ADDRESS (bit 3) - Same as above.
40	A0	ADDRESS (bit 0) - Same as above.
41	GND	GROUND
42	GND	GROUND
43	GND	GROUND

TABLE 2-2. Parallel I/O Connector Pin Assignments (J4)

PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
1	INPUT	INPUT PRIME - A low-level output signal which clears the printer buffer and initializes the logic. (Not used by all printers).
3	GND	GROUND - Printer interface ground.
5	FAULT	FAULT - A low-level input signal that indicates a printer fault condition such as paper empty, light detect, or a desselect condition. (Not used by all printers).
7	GND	GROUND - Same as pin 3.

TABLE 2-2. Parallel I/O Connector Pin Assignments (J4) (cont'd)

PIN	SIGNAL	SIGNAL NAME AND DESCRIPTION
9	PB7	PERIPHERAL DATA LINE (PB7) - Audio-cassette Receive Data.
11	PB6	PERIPHERAL DATA LINE (PB6) - Audio-cassette Transmit Data.
13	PB5	PERIPHERAL DATA LINE (PB5) - Free.
15	PB4	PERIPHERAL DATA LINE (PB4) - Free.
17	PB3	PERIPHERAL DATA LINE (PB3) - Free.
19	BUSY	BUSY - An input signal indicationg that the printer cannot receive data.
21	OUT-PP	OUT OF PAPER - A high-level input indicating the printer is out of paper.
23	SEL	SELECT - A high-level input signal indicating that the printer is selected.
25	PD8	PERIPHERAL DATA LINE (PD8) - Output data to printer from PA7 of PIA.
27	PD7	PERIPHERAL DATA LINE (PD7) - Same as pin 25 except bit A6.
29	PD6	PERIPHERAL DATA LINE (PD6) - Same as pin 25 except bit A5.
31	PD5	PERIPHERAL DATA LINE (PD5) - Same as pin 25 except bit A4.
33	PD4	PERIPHERAL DATA LINE (PD4) - Same as pin 25 except bit A3.
35	PD3	PERIPHERAL DATA LINE (PD3) - Same as pin 25 except bit A2.
37	PD2	PERIPHERAL DATA LINE (PD2) - Same as pin 25 except bit A1.
39	PD1	PERIPHERAL DATA LINE (PD1) - Same as pin 25 except bit A0.
41	GND	GROUND - Same as pin 3.
43	DATASTB	DATA STROBE - A 1.0 microsecond output pulse used to clock data from the MPU to the printer logic.
45	GND	GROUND - Same as pin 3.
47	ACKNLG	ACKNOWLEDGE - A low-level input pulse indicating the input of a character into memory or the end of a functional operation.
49	GND	GROUND - Same as pin 3.

All even numbers (2-50) : GROUND.

MATING CONNECTOR :
3M 3415-0001 or equivalent.

TABLE 2-13. EXORset Main Controller Board Jumper Options

JUMPER			FUNCTION
SW2-1 (OUT)	SW2-2 (OUT)		PIA1 data lines :
IN	X		PB6 available on J4 pin 11
X	IN		PB7 available on J4 pin 9
SW3-1 (OUT)	SW3-2 (OUT)	SW3-3 (OUT)	PIA1 B-side interrupt :
IN	OUT	OUT	to MPU NMI
OUT	IN	OUT	to MPU FIRQ
OUT	OUT	IN	to MPU IRQ
SW4-1 (IN)	SW4-2 (OUT)	SW4-3 (OUT)	ACIA interrupt :
IN	OUT	OUT	to MPU NMI
OUT	IN	OUT	to MPU FIRQ
OUT	OUT	IN	to MPU IRQ
SW5-1 (OUT)	SW5-2 (OUT)	SW5-3 (OUT)	Micromodule 11 supply :
IN	IN	IN	+5 Vdc, -12 Vdc, +12 Vdc available for Micromodule 11 on J3 pin 16, 18 and 20 respectively
SW6-1 (OUT)	SW6-2 (OUT)	SW6-3 (OUT)	PIA1 A-side interrupt :
IN	OUT	OUT	to MPU NMI
OUT	IN	OUT	to MPU FIRQ
OUT	OUT	IN	to MPU IRQ
SW7-1 (IN)	SW7-2 (OUT)	SW7-3 (OUT)	PTM interrupt :
IN	OUT	OUT	to MPU NMI
OUT	IN	OUT	to MPU FIRQ
OUT	OUT	IN	to MPU IRQ
SEE FIGURE 2-1.			RS-232C interface :
SW9 1 to 4 (IN)		SW9 2 to 3 (IN)	Graphic RAM base address :
1-4		1-3	0000
1-4		2-3	4000
2-4		1-3	8000

TABLE 2-13. EXORset Main Controller Board Jumper Options (cont'd)

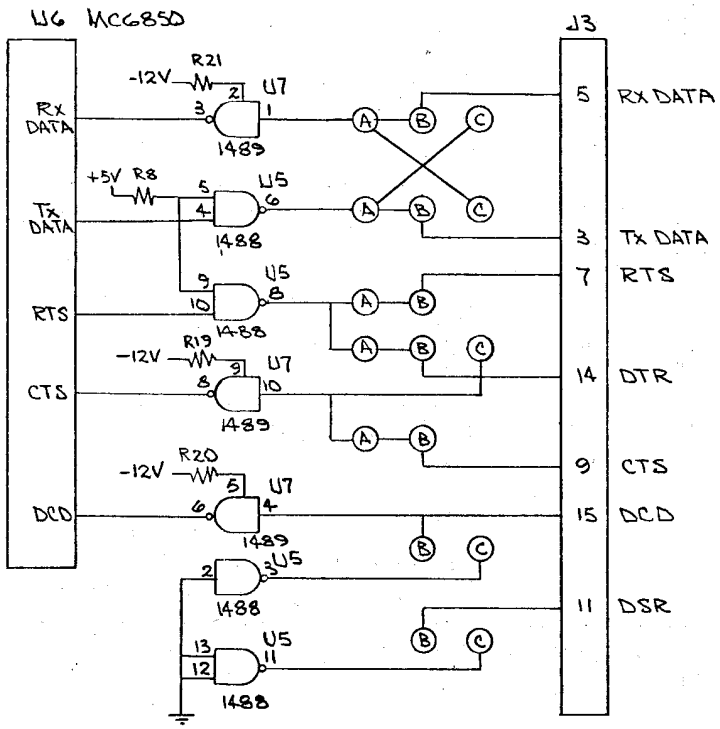
JUMPER		FUNCTION
SW10-1 (OUT)	SW10-2 (IN)	2K/4K EPROM option :
OUT	IN	2K EPROM device in socket U14
IN	OUT	4K EPROM device in socket U14
SW11-1 (OUT)	SW11-2 (IN)	2K/4K EPROM option :
OUT	IN	2K EPROM device in socket U16
IN	OUT	4K EPROM device in socket U16
SW12-1 (OUT)	SW12-2 (IN)	2K/4K EPROM option :
OUT	IN	2K EPROM device in socket U18
IN	OUT	4K EPROM device in socket U18
SW13-1 (OUT)	SW13-2 (IN)	2K/4K EPROM option :
OUT	IN	2K EPROM device in socket U20
IN	OUT	4K EPROM device in socket U20
SW14-1 (OUT)	SW14-2 (IN)	2K/4K EPROM option :
OUT	IN	2K EPROM device in socket U31
IN	OUT	4K EPROM device in socket U31
SW15-1 (OUT)	SW15-2 (IN)	2K/4K EPROM option :
OUT	IN	2K EPROM device in socket U22
IN	OUT	4K EPROM device in socket U22
SW16-1 (OUT)	SW16-2 (IN)	2K/4K EPROM option :
OUT	IN	2K EPROM device in socket U33
IN	OUT	4K EPROM device in socket U33
SW17-1 (OUT)	SW17-2 (IN)	Address decode PROMs select :
IN	OUT	PROM chip select to GND
OUT	IN	PROM only selected during MPU access

TABLE 2-13. EXORset Main Controller Board Jumper Options (cont'd)

JUMPER			FUNCTION
SW18-1 (OUT)	SW18-2 (OUT)	SW18-3 (OUT)	EXORset initialization at power-up :
OUT	X	X	80 characters / line display
IN	X	X	40 characters / line display
X	OUT	X	50 Hz (EUR)
X	IN	X	60 Hz (USA)
X	X	OUT	MAP 1
X	X	IN	MAP 2
SW19-1 (OUT)	SW19-2 (IN)	SW19-3 (OUT)	PIA3 A-side interrupt :
IN	OUT	OUT	to MPU FIRQ
OUT	IN	OUT	to MPU NMI
OUT	OUT	IN	to MPU IRQ
SW20-1 (OUT)	SW20-2 (OUT)	SW20-3 (OUT)	PIA3 B-side interrupt :
IN	OUT	OUT	to MPU FIRQ
OUT	IN	OUT	to MPU NMI
OUT	OUT	IN	to MPU IRQ
SW21-1 (OUT)	SW21-2 (OUT)	SW21-3 (OUT)	Keyboard encoder language selection :
OUT	OUT	OUT	English
IN	IN	OUT	Spanish
OUT	OUT	IN	German
IN	OUT	IN	Swedish
OUT	IN	IN	Norwegian / Danish
IN	IN	IN	French
			NOTE : for languages other than english (standard), the character generator and the keyboard key tops must be changed accordingly.
SW22-1 (OUT)	SW22-2 (OUT)	SW22-3 (IN)	PIA2 B-side interrupt :
IN	OUT	OUT	to MPU IRQ
OUT	IN	OUT	to MPU FIRQ
OUT	OUT	IN	to MPU NMI
SW23-1 (OUT)	SW23-2 (OUT)	SW23-3 (IN)	PIA2 A-side interrupt :
IN	OUT	OUT	to MPU IRQ
OUT	IN	OUT	to MPU FIRQ
OUT	OUT	IN	to MPU NMI

TABLE 2-13. EXORset Main Controller Board Jumper Options (cont'd)

JUMPER			FUNCTION
SW24-1 (OUT)	SW24-2 (IN)		Audio-cassette playback signal phase selection:
IN	OUT		playback signal not inverted
OUT	IN		playback signal inverted
			NOTE : some cassette recorders invert the recorded signal, therefore jumper SW24 allows for proper phase recovering
SW25-1 (OUT)	SW25-2 (OUT)	SW25-3 (OUT)	Non-standard bus signals :
OUT	OUT	OUT	RAS', CAS', EAHL' to J07 only
IN	IN	IN	RAS', CAS', EAHL' to J07, J08, J09



EXORset as a terminal to a host (EXORciser):
As delivered - printed wire between point A & point B .

EXORset as a modem to a terminal:
Cut printed wire between point A & point B .
Add jumper from point B to point C .

FIGURE 2-1. RS-232C Interface Jumper Options

TABLE 2-14. EXORset Mini-Floppy Disk Controller Board Jumper Options

SWA-1 (OUT)				Low current signal :
IN				to P2 pin 34 (provision for norm. drives)
OUT				if mini-floppy drives are used
SWA-2 (OUT)				Optional drive 3 :
IN				SELECT3 signal to P2 pin 4
OUT				not connected
SWA-5 (OUT)	SWA-6 (IN)			FDC clock select :
IN	OUT			1 MHz clock to FDC (provision for normal drive)
OUT	IN			500 KHz clock to FDC (mini-floppy)
SWA-7 (OUT)	SWA-8 (IN)			MEMCLK / E select :
IN	OUT			MEMCLK signal to FDC / clock divider
OUT	IN			E signal to clock divider
				16K RAM base address select :
SWB-4 (OUT)	SWB-3 (IN)	SWB-2 (IN)	SWB-1 (OUT)	
IN	OUT	IN	OUT	0000
IN	OUT	OUT	IN	4000
OUT	IN	IN	OUT	8000
OUT	IN	OUT	IN	C000

TABLE 2-14. EXORset Mini-Floppy Disk Controller Board Jumper Options (cont'd)

FDC and disk driver base address :

SWC-8 (OUT)	SWC-7 (IN)	SWC-6 (OUT)	SWC-5 (IN)	SWC-4 (OUT)	SWC-3 (IN)	SWC-2 (IN)	SWC-1 (OUT)	
IN	OUT	IN	OUT	IN	OUT	IN	OUT	0000
IN	OUT	IN	OUT	IN	OUT	OUT	IN	1000
IN	OUT	IN	OUT	OUT	IN	IN	OUT	2000
IN	OUT	IN	OUT	OUT	IN	OUT	IN	3000
IN	OUT	OUT	IN	IN	OUT	IN	OUT	4000
IN	OUT	OUT	IN	IN	OUT	OUT	IN	5000
IN	OUT	OUT	IN	OUT	IN	IN	OUT	6000
IN	OUT	OUT	IN	OUT	IN	OUT	IN	7000
OUT	IN	IN	OUT	IN	OUT	IN	OUT	8000
OUT	IN	IN	OUT	IN	OUT	OUT	IN	9000
OUT	IN	IN	OUT	OUT	IN	IN	OUT	A000
OUT	IN	IN	OUT	OUT	IN	OUT	IN	B000
OUT	IN	OUT	IN	IN	OUT	IN	OUT	C000
OUT	IN	OUT	IN	IN	OUT	OUT	IN	D000
OUT	IN	OUT	IN	OUT	IN	IN	OUT	E000
OUT	IN	OUT	IN	OUT	IN	OUT	IN	F000

SWD-1 (OUT)	SWD-2 (IN)	READY select :
IN	OUT	READY generated on-board (for drives without READY signal)
OUT	IN	READY signal from the drive

Map assignment :

SWD-3 (OUT)	SWD-4 (OUT)	SWD-7 (OUT)	SWD-8 (IN)	
IN	OUT	IN	OUT	FDC and disk driver in map 1 16K RAM in map 2
IN	OUT	OUT	IN	FDC and disk driver in map 2 16K RAM in map 1
OUT	IN	IN	OUT	FDC and disk driver in map 2 16K RAM in map 2
OUT	IN	OUT	IN	FDC and disk driver in map 1 16K RAM in map 1
OUT	OUT	X	X	FDC and disk driver respond in both maps 16K RAM in map 1 or 2 (depending on SWD-7 and SWD8)
X	X	OUT	OUT	FDC and disk driver in map 1 or 2 (depending on SWD-3 and SWD-4) 16K RAM responds in both maps

2.6 USE AS A TERMINAL

The user has the option of connecting the EXORset to a RS-232C compatible device (e.g. an EXORciser). The switch SW4-1 must be installed (selecting NMI) for the EXORbug commands to work. To connect the EXORset to a 20 mA current loop device, use the Micromodule M68MM11 (RS-232C to TTY adapter). Refer to the M68MM11 manual for installation.

For a description of the signals available on the RS-232C connector, refer to Table 2-3.

The necessary cable is a 25-conductor flat cable with a 3M-3461-0001, 2 x 10-pin card edge connector (or equivalent) at the EXORset end (conductors 21 to 25 not used) and ANSLEY 501-659-2, 25-pin connector (or equivalent) at the peripheral end.

To switch the EXORset from the stand-alone mode of operation (off-line) to the terminal mode of operation (on-line), enter the command :

XCOM C/R

To switch the EXORset from the terminal mode of operation (on-line) to the stand-alone mode of operation (off-line), enter the sequence :

ESC-0

Note that this command works only if it is echoed from the host computer.

This serial port is also used by the DWLD and DUMP commands to transfer the contents of memory from, and to, the Host. See paragraph 5.2.10 for other details.

2.7 TESTING HARDWARE/SOFTWARE INTERFACES

The EXORset is limited to three module slots so it is not possible to emulate a system in the same way as with an EXORciser, but it is possible to evaluate I/O routines for fairly complex systems. Two module slots are always available and, in special cases, a third one can be used (by using cassette instead of the minifloppies). For example, one or a combination of the following modules can be used:

MEX6820	I/O module
MEX6850	ACIA module
M68MM07	Quad ACIA/SSDA micromodule
M68MM12	IEEE micromodule
M68MM13	Digital interface micromodules
M68MM05	A/D, D/A micromodules
M68MM15	A/D, D/A micromodules

The list is not limited to this, and it is also to be noted that EXORset has a PIA, ACIA, and PIA and numerous EROM sockets which can be used to emulate Micromodule 19 and/or Micromodule 4. The modules with VUA enabling will respond in map 2 and, if they can select VXA, they will be in map 1.

As can be seen in Figure 5-3, the standard EXORset (with standard address decoding) has space at EC10 to EF00 for these added I/O devices. Table 5-4 gives the addresses of the built-in PTM, ACIA, and PIA which can be used to emulate Micromodule 19, for example. Tables 5-1, 5-2, and 5-3 give the addresses of various EROM sockets. Paragraph 2.8 explains how these address PROM's can be changed if more exacat emulation is required.

Another factor is whether or not the routines and hardware use interrupts. The I/O modules have provision to connect IRQ; bit if FIRQ or NMI were to be required, it will be necessary to install a jumper on the module.

NOTE

The user is cautioned to be careful about trying to solder to the gold-plated fingers of the connector, since the solder may run all over the contact unless properly done. The board should be oriented with the connector up and only a very little solder used.

When using interrupts for I/O, it will be necessary to set up a user vector table with second level interrupts, and to change the ATOP vector as described in paragraph 4.4.

When emulating certain system configurations, it may be necessary to change the interrupt connections for EXORset ACIA or PIA1. These are determined by jumpers on SW3, SW4, and SW6. SW4-1 is normally jumpered to NMI to allow the EXORbug commands of XCOM, DWLD, and DUMP to work properly. It is recommended that this jumper be cut and a DIP switch be installed in these locations to allow NMI, IRQ, or FIRQ to be switchable. IRQ or FIRQ would be used in a typical system.

2.8 USER-DEFINED ADDRESS MAP

The various memory blocks and I/O devices are decoded using fusible-link PROM's. By reprogramming these PROM's, any configuration of RAM, E/ROM, I/O devices can be redefined, in 256-byte increments. The maximum available address space is 56K bytes in each map. The upper 8K address range is reserved for the system. Tables 5-1, 5-2, and 5-3 in Chapter 5 show the address decode PROM contents corresponding to the EXORset standard memory map. An example is given in paragraph 5.2.4 describing how to define a new address map.

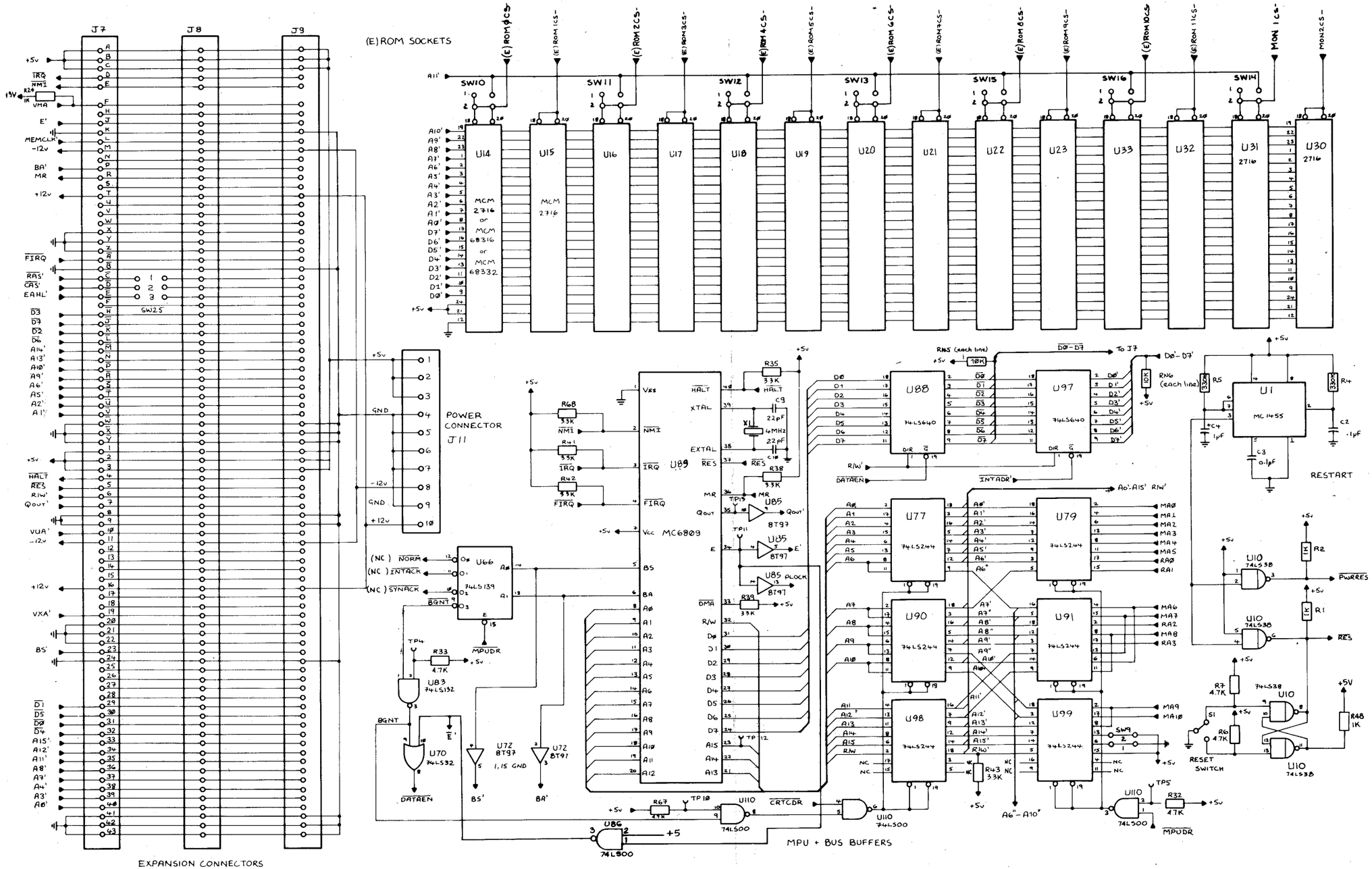


FIGURE 7-1. Main Controller Board Schematic Diagram (Sheet 1 of 3)

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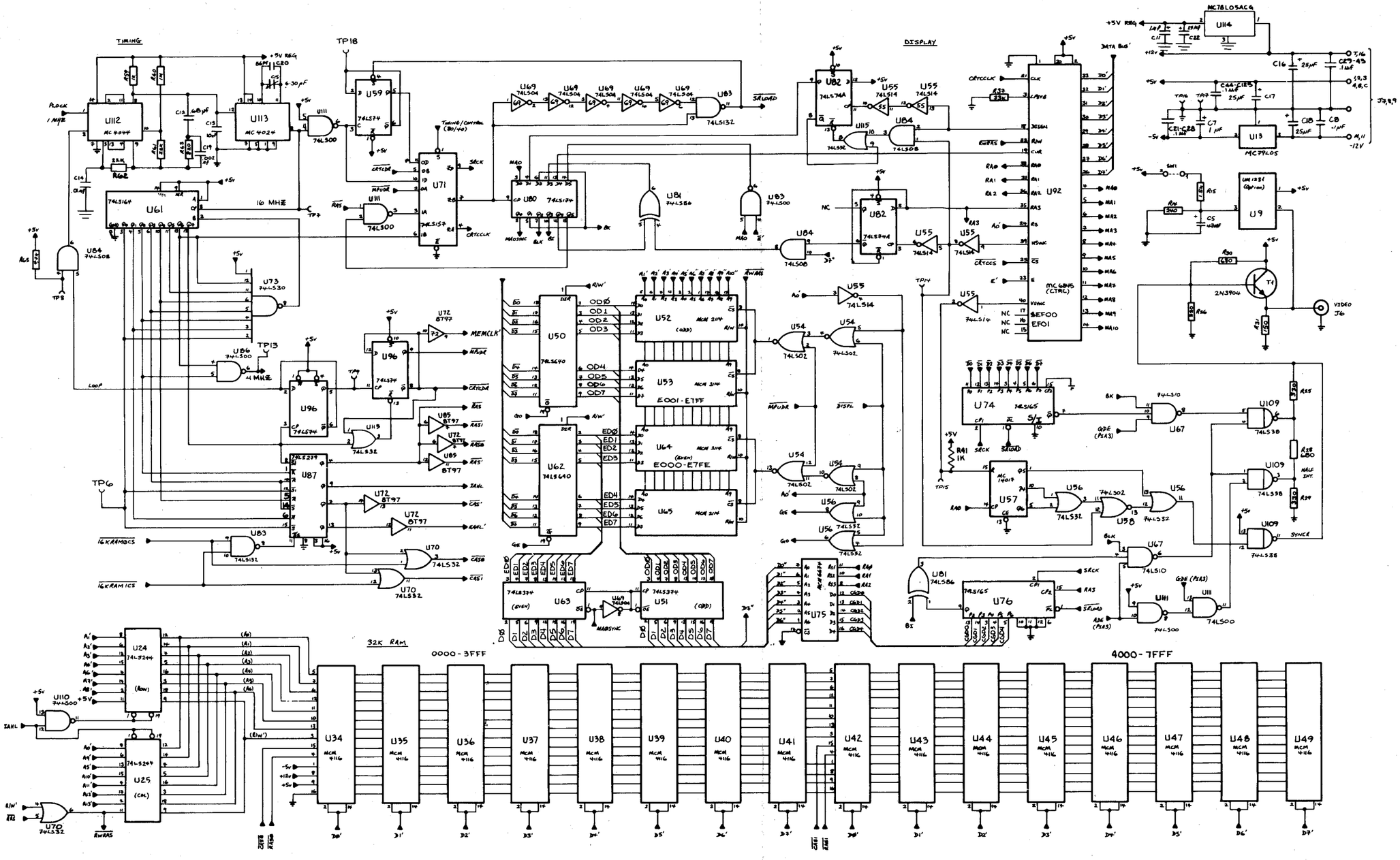

FIGURE 7-1. Main Controller Board Schematic Diagram (Sheet 2 of 3)

63EW1215B Rev. A 7-5/7-6

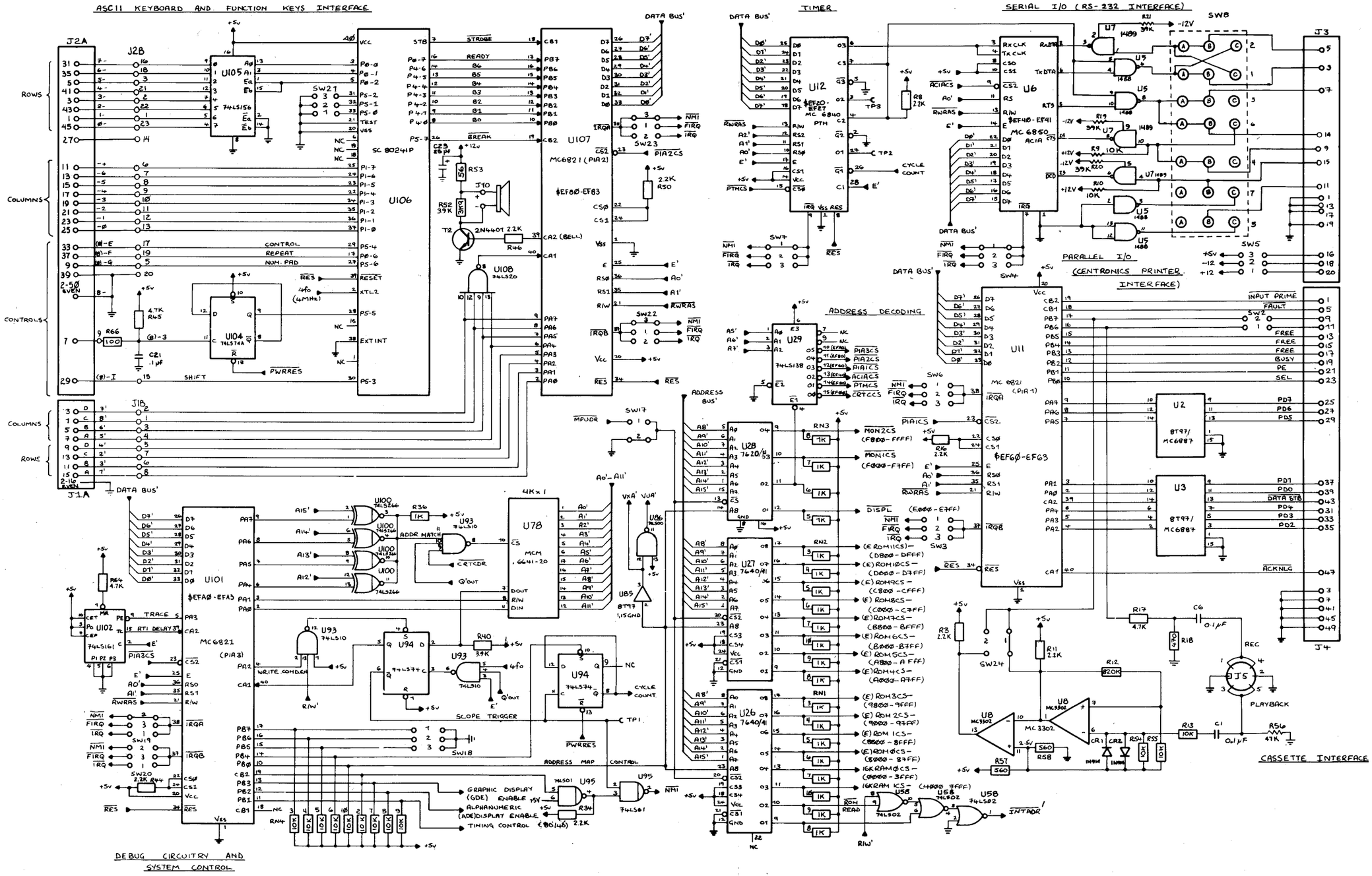

FIGURE 7-1. Main Controller Board Schematic Diagram (Sheet 3 of 3)

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FIGURE 7-2. Floppy Disc Controller Board Schematic

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