SN74AHCT367 Hex Buffer and Line Driver with 3-State Output

1 Features

- Inputs are TTL-Voltage Compatible
- True Outputs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 200-V Machine Model
  - 2000-V Charged-Device Model

2 Applications

- Telecom Infrastructure
- TVs
- Set Top Boxes
- Network Switches
- Wireless Infrastructure
- Electronic Points of Sale

3 Description

The SN74AHCT367 device is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

Device Information(1)

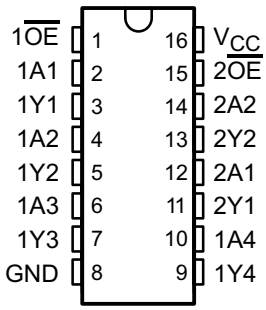
PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AHCT367	PDIP (16)	19.30 mm x 6.35 mm
	SSOP (16)	6.50 mm x 5.30 mm
	TSSOP (16)	5.00 mm x 4.40 mm
	SOP (16)	10.20 mm x 5.30 mm
	SOIC (16)	9.00 mm x 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

6 Pin Configuration and Functions

SN74AHCT367 . . . D, DB, DGV, OR PW PACKAGE
(TOP VIEW)



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	$1\overline{OE}$	I	Output Enable 1
2	1A1	I	1A1 Input
3	1Y1	O	1Y1 Output
4	1A2	I	1A2 Input
5	1Y2	O	1Y2 Output
6	1A3	I	1A3 Input
7	1Y3	O	1Y3 Output
8	GND	—	Ground Pin
9	1Y4	O	1Y4 Output
10	1A4	I	1A4 Input
11	2Y1	O	2Y1 Output
12	2A1	I	2A1 Input
13	2Y2	O	2Y2 Output
14	2A2	I	2A2 Input
15	$2\overline{OE}$	I	Output Enable 2
16	V_{CC}	—	Power Pin